32-Channel, 14-Bit DAC with Full-Scale Output Voltage Programmable from 50 V to 200 V

Preliminary Technical Data

AD5535

FEATURES

High integration: 32-channel, 14-bit DAC with integrated, high voltage output amplifier

Guaranteed monotonic

Housed in 15 × 15 mm CSP-BGA package

Full-scale output voltage programmable from 50 V to 200 V via reference input

700 µA drive capability

Integrated silicon diode for temperature monitoring

DSP-/microcontroller-compatible serial interface

Channel update rate: 1.2 MHz

Asynchronous $\overline{\text{RESET}}$ facility

Temperature range: –10°C to +85°C

APPLICATIONS

Optical micro-electromechanical systems (MEMS)

Optical cross-point switches

Micropositioning applications using Piezo Flextures

Level setting in automotive test and measurement

GENERAL DESCRIPTION

The AD5535 is a 32-channel, 14-bit DAC with an on-chip high voltage output amplifier. This device is targeted for optical micro-electromechanical systems. The output voltage range is programmable via the REFIN pin. Output range is 0 V to 50 V with REFIN = 1 V and is 0 V to 200 V with REFIN = 4 V. Each amplifier can source 700 µA, which is ideal for the deflection and control of optical MEMS mirrors.

The selected DAC register is written to via the 3-wire interface. The serial interface operates at clock rates of up to 30 MHz and is compatible with DSP and microcontroller interface standards.

The device is operated with AV_{CC} = 4.75 to 5.25 V, DV_{CC} = 2.7 V to 5.25 V, V_- = −4.75 V to −5.25 V, V+ = +4.75 V to +5.25 V, V_{PP} = 210 V. REF_IN is buffered internally on the AD5535 and should be driven from a stable reference source.

FUNCTIONAL BLOCK DIAGRAM

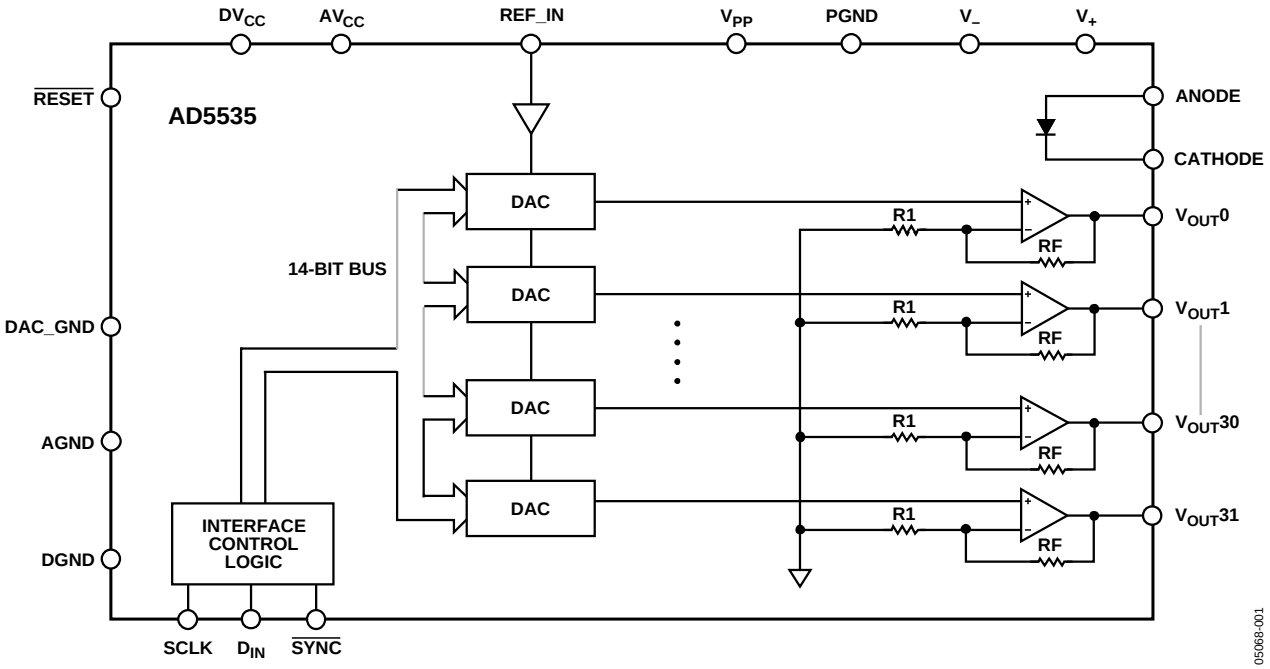

Figure 1.

Rev. PrE

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REVISION HISTORY

10/04—Revision PrE: Preliminary Version

SPECIFICATIONS

V_{PP} = 210 V, V_- = −5 V, V_+ = +5 V; AV_{CC} = 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 4.096 V; all outputs unloaded. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Grade[2]				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE					
Resolution		14		Bits	
Integral Nonlinearity (INL)		±0.1		% of FSR	
Differential Nonlinearity (DNL)		±0.5	±1	LSB	Guaranteed monotonic
Zero Code Voltage			2	V	
Offset Error	–45		+45	mV	
Offset Drift		0.09		LSB/°C	
Voltage Gain	47.5	50	52.5	V/V	
Gain Temperature Coefficient		TBD		ppm/°C	
Channel-to-Channel Gain Match		5		%	
Full-Scale Voltage Drift		8		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range[3]	0		V_{PP} – 10	V	
Output Impedance		50		Ω	
Resistive Load[4, 5]	1			MΩ	
Capacitive Load[4]			200	pF	
Short-Circuit Current		0.7		mA	
DC Crosstalk[4]			3	LSB	
DC Power Supply Rejection (PSRR), V_{PP}		70		dB	
AC CHARACTERISTICS					
Settling Time					
1/4 to 3/4 Scale Step		30		µs	No load
		100		µs	200 pF load
1 LSB Step		10		µs	No load
		10		µs	200 pF load
Slew Rate		10		V/µs	No load
		3		V/µs	200 pF load
–3 dB Bandwidth	5			kHz	
Output Noise Spectral Density		TBD		nV/√Hz	Measured at 1 kHz
0.1 Hz to 10 Hz Output Noise Voltage		TBD		µV p-p	
Digital-to-Analog Glitch Impulse		TBD		nV–s typ	1 LSB change around major carry
Digital Crosstalk		TBD		nV–s typ	
Analog Crosstalk		13		µV–s typ	
Digital Feedthrough		TBD		nV–s typ	
VOLTAGE REFERENCE, REF_IN[6]					AV_{CC} must exceed REFIN by 1.25 V min
Input Voltage Range[4]	1		4.096	V	
Input Current			1	µA	
TEMPERATURE MEASUREMENT DIODE[4]					
Peak Inverse Voltage, P_{IV}			5	V	Cathode to anode
Forward Diode Drop, V_F			0.8	V	I_F = 2 mA, anode to cathode
Forward Diode Current, I_F			2	mA	Anode to cathode
V_F Temperature Coefficient, T_C		–1.44		mV/°C	I_F = 250 µA

Parameter[1]	A Grade[2] Min	Typ	Max	Unit	Conditions/Comments
DIGITAL INPUTS[4]					
Input Current		±5	±10	µA	
Input Low Voltage			0.8	V	DV_{CC} = 3 V to 5 V
Input High Voltage	2.0			V	DV_{CC} = 3 V to 5 V
Input Hysteresis (SCLK and $\overline{SYNC}$ only)		200		mV	
Input Capacitance			10	pF	
POWER-SUPPLY VOLTAGES					
V_{PP}	(50 × REF_IN) +10	210	225	V	
V_-	−5.25		−4.75	V	
V_+	4.75		5.25	V	
AV_{CC}	4.75		5.25	V	
DV_{CC}	2.7		5.25	V	
POWER-SUPPLY CURRENTS[7]					
I_{PP}		75	110	µA/channel	
I_-		2.5	3.5	mA	
I_+		2.5	3.5	mA	
AI_{CC}		16	20	mA	
DI_{CC}		0.1	0.5	mA	
POWER DISSIPATION		609		mW	

[1] See Terminology.
[2] A Grade temperature range: −10°C to +85°C; typically +25°C.
[3] Linear output voltage range: +7 V to V_{PP} − 10 V.
[4] Guaranteed by design and characterization, not production tested.
[5] Ensure that T_J max is not exceeded. See the Absolute Maximum Ratings section.
[6] Reference input determines output voltage range. Using a 4.096 V reference (REF 198) gives an output voltage range of 0 V to 200 V. Output range is programmable via the reference input. The full-scale output range is programmable from 50 V to 200 V. The linear output voltage range is restricted from 7 V to V_{PP} − 10 V.
[7] Outputs unloaded.

TIMING CHARACTERISTICS

V_{PP} = 210 V, V_- = −5 V, V_+ = +5 V; AV_{CC} = 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 4.096 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1, 2, 3]	A Grade	Unit	Conditions/Comments
f_{UPDATE}	1.2	MHz max	Channel Update Rate
f_{CLKIN}	30	MHz max	SCLK Frequency
t_1	13	ns min	SCLK High Pulse Width
t_2	13	ns min	SCLK Low Pulse Width
t_3	15	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	50	ns min	$\overline{SYNC}$ Low Time
t_5	10	ns min	$\overline{SYNC}$ High Time
t_6	10	ns min	DIN Setup Time
t_7	5	ns min	DIN Hold Time
t_8	200	ns min	19th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge for Next Write
t_9	20	ns min	$\overline{RESET}$ Pulse Width

[1] See timing diagrams in Figure 2.
[2] Guaranteed by design and characterization, not production tested.
[3] All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

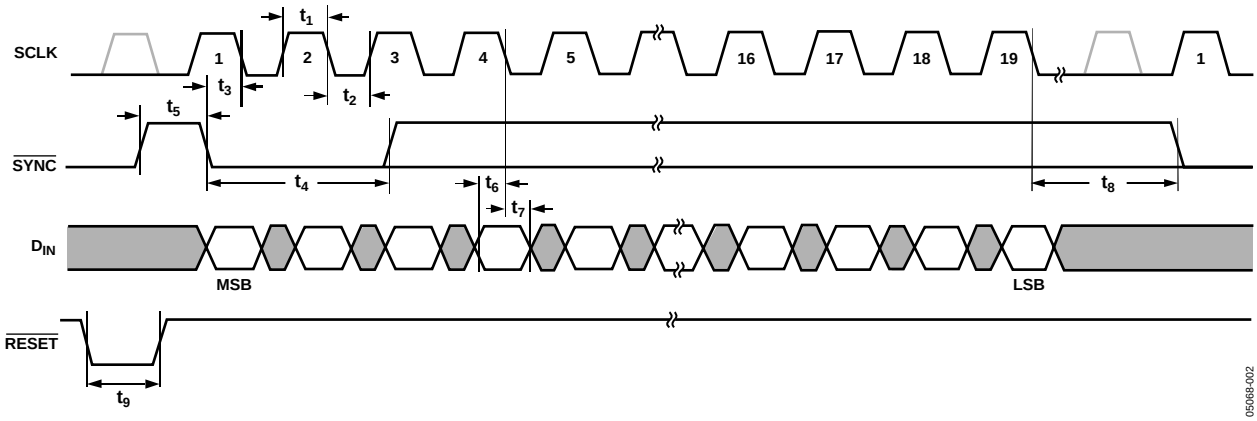

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{PP} to AGND	0.3 V to 225 V
V_- to AGND	+0.3 V to −6 V
V_+ to AGND	−0.3 V to +7 V
AV_{CC} to AGND, DAC_GND	−0.3 V to +7 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
REF_IN to AGND, DAC_GND	−0.3 V to AV_{CC} + 0.3 V
V_{OUT} 0–31 to AGND	V_- to V_{PP}
Anode/Cathode to AGND, DAC_GND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range	
Industrial	−10°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
124-Lead CSP-BGA Package, θ_{JA} Thermal Impedance	40°C/W
Reflow Soldering	
Peak Temperature	220°C
Time at Peak Temperature	10 s to 40 s

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Transient currents up to 100 mA do not cause SCR latch-up.

This device is a voltage-integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

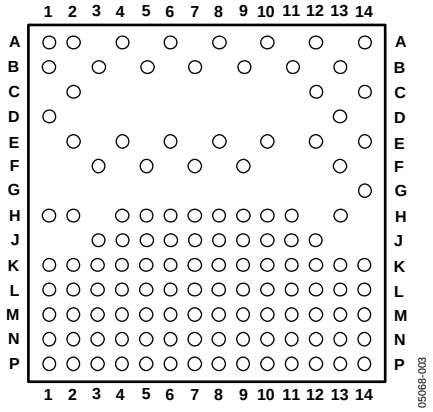

Figure 3. Pin Configuration

Table 4. 124-Lead CSP-BGA Ball Configuration

CSP-BGA Number	Ball Name
A1	N/C
A2	V_{OUT} 1
A4	V_{OUT} 7
A6	V_{OUT} 11
A8	V_{OUT} 16
A10	V_{OUT} 20
A12	V_{OUT} 25
A14	N/C
B1	V_{OUT} 0
B3	V_{OUT} 4
B5	V_{OUT} 9
B7	V_{OUT} 13
B9	V_{OUT} 17
B11	V_{OUT} 21
B13	V_{OUT} 26
C2	V_{OUT} 3
C12	V_{OUT} 22
C14	V_{OUT} 29
D1	V_{OUT} 2
D13	V_{OUT} 23
E2	V_{OUT} 5
E4	V_{OUT} 8
E6	V_{OUT} 12
E8	V_{OUT} 15
E10	V_{OUT} 19
E12	V_{OUT} 24
E14	V_{OUT} 31
F3	V_{OUT} 6
F5	V_{OUT} 10
F7	V_{OUT} 14
F9	V_{OUT} 18
F13	V_{OUT} 30
G14	V_{OUT} 28
H1	V_{PP}
H2	V_{PP}
H13	V_{OUT} 27
J3–J12	AGND
K1	V_+
K2	V_+
K3–K14	AGND
L1	V_-
L2	V_-
L3–L13	AGND
L14	DAC_GND
M1	AGND
M2	AGND
M3–12	AGND
M13	AV_{CC}
M14	AV_{CC}
N1	PGND
N2	PGND
N3	CATHODE
N4	ANODE
N5–N14	AGND
P1	N/C
P2	REF_IN
P3	DAC_GND
P4	$\overline{\text{RESET}}$
P5	DV_{CC}
P6	DGND
P7	TEST
P8	D_{IN}
P9	SCLK
P10	$\overline{\text{SYNC}}$
P11–P13	AGND
P14	N/C

Table 5. Pin Function Descriptions

Pin	Function
AGND	Analog GND Pins.
AV_{CC}	Analog Supply Pins. Voltage range from 4.75 V to 5.25 V.
V_{PP}	Output Amplifier High Voltage Supply. Voltage range from (REF_IN × 50) + 10 V to 225 V.
V_+	V_+ Amplifier Supply Pins. Voltage range from 4.75 V to 5.25 V.
V_-	V_- Amplifier Supply Pins. Voltage range from −4.75 V to −5.25 V.
PGND	Output Amplifier Ground Reference Pins.
DGND	Digital GND Pins.
DV_{CC}	Digital Supply Pins. Voltage range from 2.7 V to 5.25 V.
DAC_GND	Reference GND Supply for All the DACs.
REF_IN	Reference Voltage for Channels 0–31. Reference input range is 1 V to 4 V and can be used to program the full-scale output voltage from 50 V to 200 V.
V_{OUT} (0–31)	Analog Output Voltages from the 32 Channels.
ANODE	Anode of Internal Diode for Diode Temperature Measurement.
CATHODE	Cathode of Internal Diode for Diode Temperature Measurement.
$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
SCLK[1]	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds of up to 30 MHz.
D_{IN}[1]	Serial Data Input. Data must be valid on the falling edge of SCLK.
TEST	Allows the same data to be simultaneously loaded to all channels of the AD5535. This pin is used for calibration purposes when loading zero scale and full scale to all channels. To invoke this feature, take the TEST pin high. In normal operation, TEST should be tied low.
$\overline{RESET}$[1]	Active Low Input. This pin can also be used to reset the complete device to its power-on reset conditions. Zero code is loaded to the DACs.

[1] Internal pull-up device on this logic input. Therefore, it can be left floating and defaults to a logic high condition.

TERMINOLOGY

Integral Nonlinearity (INL)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of full-scale range.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Zero-Code Voltage
A measure of the output voltage present at the device output with all 0s loaded to the DAC. It includes the offset of the DAC and the output amplifier. It is expressed in V.

Offset Error
Calculated by taking two points in the linear region of the transfer function, drawing a line through these points, and extrapolating back to the Y axis. It is expressed in mV.

Voltage Gain
Calculated from the change in output voltage for a change in code multiplied by 16,384 and divided by the REF_IN voltage. This is calculated between two points in the linear section of the transfer function.

Gain Error
A measure of the output error with all 1s loaded to the DAC, and is the difference between the ideal and actual analog output range. Ideally, the output should be 50 × REF_IN. It is expressed as a percentage of full-scale range.

DC Power-Supply Rejection Ratio (PSRR)
A measure of the change in analog output for a change in V_{PP} supply voltage. It is expressed in dB. V_{PP} is varied ±5%.

DC Crosstalk
The dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and the output change of all other DACs. It is expressed in LSB.

Output Temperature Coefficient
A measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

Output Voltage Settling Time
The time taken from when the last data bit is clocked into the DAC until the output has settled to within ±0.5 LSB of its final value.

Digital-to-Analog Glitch Impulse
The area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV–s, when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Crosstalk
The glitch impulse transferred to the output of one DAC at midscale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV–s.

Analog Crosstalk
The area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV–s.

Digital Feedthrough
A measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to ($\overline{SYNC}$ is high). It is specified in nV–s and is measured with a worst-case change on the digital input pins, for example, from all 0s to all 1s and vice versa.

Output Noise Spectral Density
A measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(Hz)^{1/2}$.

TYPICAL PERFORMANCE CHARACTERISTICS

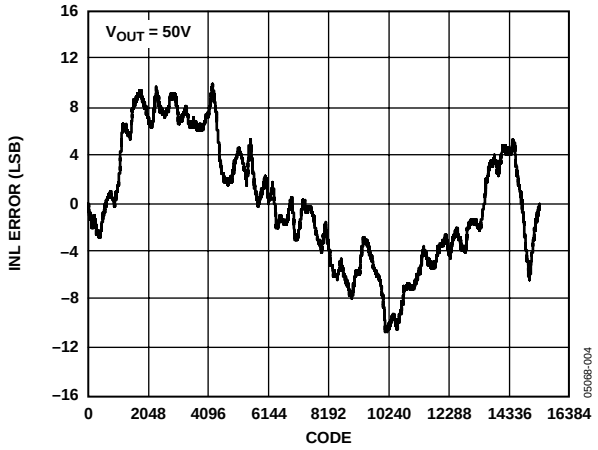

Figure 4. Integral Linearity with V_{PP} = 60 V, V_{OUT} Full Scale = 50 V

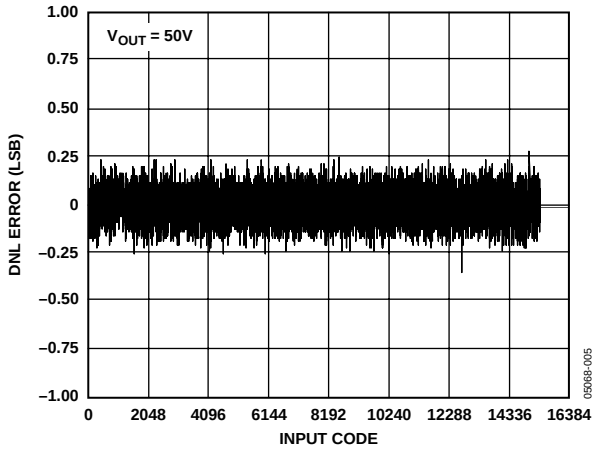

Figure 5.DNL with V_{PP} = 60 V, V_{OUT} Full Scale = 50 V

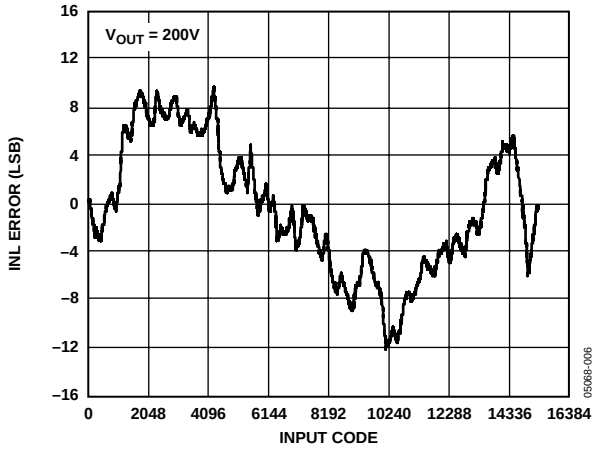

Figure 6. Integral Linearity with V_{PP} = 210 V, V_{OUT} Full Scale = 200 V

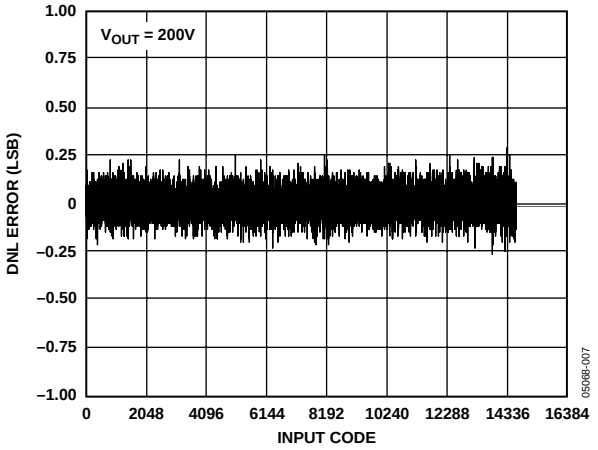

Figure 7. DNL with V_{PP} = 210 V, V_{OUT} Full Scale = 200 V

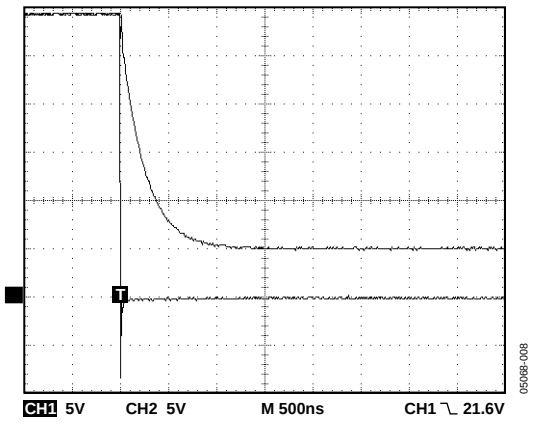

Figure 8. Short-Circuit Current Limit Timing

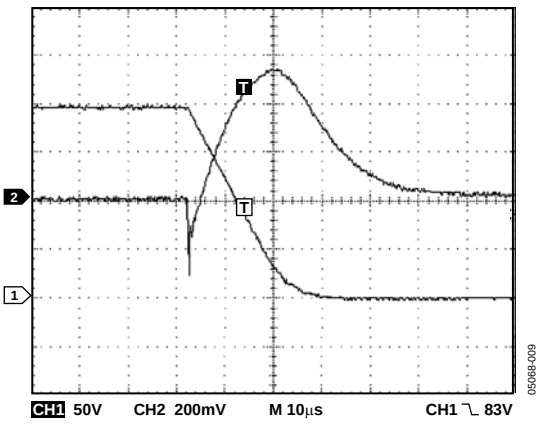

Figure 9. Worst-Case Adjacent Channel Crosstalk

FUNCTIONAL DESCRIPTION

The AD5535 consists of 32 14-bit DACs with 200 V high voltage amplifiers in a single 15 mm × 15 mm CSP-BGA package. The output voltage range is programmable via the REFIN pin. Output range is 0 V to 50 V with REFIN = 1 V, and 0 V to 200 V with REFIN = 4 V. Communication to the device is through a serial interface operating at clock rates of up to 30 MHz and is compatible with DSP and microcontroller interface standards. A 5-bit address and a 14-bit data-word are loaded into the AD5535 input register via the serial interface. The channel address is decoded, and the data-word is converted into an analog output voltage for this channel.

At power-on, all the DAC registers are loaded with 0s.

DIGITAL-TO-ANALOG SECTION

The architecture of each DAC channel consists of a resistor string DAC followed by an output buffer amplifier operating with a nominal gain of 50. The voltage at the REF_IN pin provides the reference voltage for the corresponding DAC. The input coding to the DAC is straight binary and the ideal DAC output voltage is given by

$$V_{OUT} = \frac{50 \times V_{REF\_IN} \times D}{2^{14}}$$

where *D* is the decimal equivalent of the binary code, which is loaded to the DAC register (0 to 16,383).

The output buffer amplifier is specified to drive a load of 1 MΩ and 200 pF. The linear output voltage range for the output amplifier is from 7 V to V_{PP} − 10V. The amplifier output bandwidth is typically 5 kHz, and is capable of sourcing 700 μA and sinking 2.8mA. Settling time for a full-scale step is typically 30 μs with no load and 110 μs with a 200 pF load.

RESET FUNCTION

The reset function on the AD5535 can be used to reset all nodes on the device to their power-on reset condition. All the DACs are loaded with 0s and all registers are cleared. The reset function is implemented by taking the $\overline{\text{RESET}}$ pin low.

SERIAL INTERFACE

The serial interface is controlled by three pins:

- $\overline{\text{SYNC}}$ is the frame synchronization pin for the serial interface.
- SCLK is the serial clock input. This pin operates at clock speeds of up to 30 MHz.
- D_{IN} is the serial data input. Data must be valid on the falling edge of SCLK.

To update a single DAC channel, a 19-bit data-word is written to the AD5535 input register.

A4 to A0 Bits

These bits can address any one of the 32 channels. A4 is the MSB of the address; A0 is the LSB.

DB13 to DB0 Bits

These bits are used to write a 14-bit word into the addressed DAC register.

Figure 2 is the timing diagram for a serial write to the AD5535. The serial interface works with both a continuous and a discontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{\text{SYNC}}$ are ignored until the correct number of bits are shifted in. Once 19 bits have been shifted in, the SCLK is ignored. For another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$. The user must allow 200 ns (minimum) between successive writes.

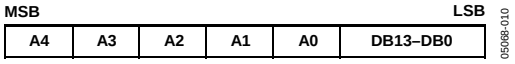

Figure 10. Serial Data Format

MICROPROCESSOR INTERFACING

AD5535 to ADSP-21xx Interface

The ADSP-21xx family of DSPs is easily interfaced to the AD5535 without the need for extra logic. A data transfer is initiated by writing a word to the TX register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5535 on the falling edge of its SCLK. The easiest way to provide the 19-bit data-word required by the AD5535, is to transmit two 10-bit data-words from the ADSP-21xx. Ensure that the data is positioned correctly in the TX register so that the first 19 bits transmitted contain valid data.

Set up the SPORT control register as follows:

TFSW = 1, Alternate Framing

INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

ISCLK = 1, Internal Serial Clock

TFSR = 1, Frame Every Word

ITFS = 1, Internal Framing Signal

SLEN = 1001, 10-Bit Data Word

Figure 11 shows the connection diagram.

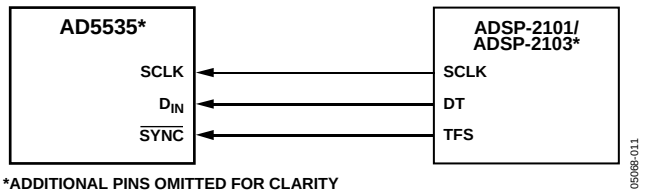

Figure 11. AD5535 to ADSP-2101/ADSP-2103 Interface

AD5535 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), clock polarity bit (CPOL) = 0, and clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR)—see the *68HC11 User Manual.* SCK of the 68HC11 drives the SCLK of the AD5535 and the MOSI output drives the serial data line (DIN) of the AD5535. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5535, the $\overline{\text{SYNC}}$ line is taken low (PC7).

Data appearing on the MOSI output is valid on the falling edge of SCK. The 68HC11 transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are necessary to transmit 19 bits of data. Data is transmitted MSB first. It is important to left-justify the data in the SPDR register so that the first 19 bits transmitted contain valid data. PC7 must be pulled low to start a transfer. It is taken high and pulled low again before any further write cycles can take place. See Figure 12.

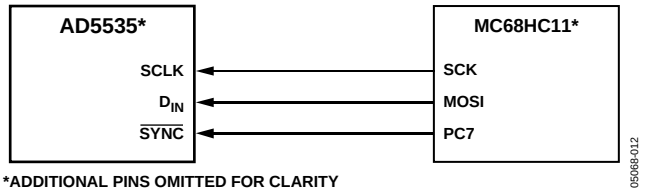

Figure 12. AD5535 to MC68HC11 Interface

AD5535 to PIC16C6X/7X

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example, I/O port RA1 is being used to pulse $\overline{\text{SYNC}}$ and enable the serial port of the AD5535. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are necessary to transmit 19 bits of data. Data is transmitted MSB first. It is important to left-justify the data in the SPDR register so that the first 19 bits transmitted contain valid data. RA1 must be pulled low to start a transfer. It is taken high and pulled low again before any further write cycles can take place. Figure 13 shows the connection diagram.

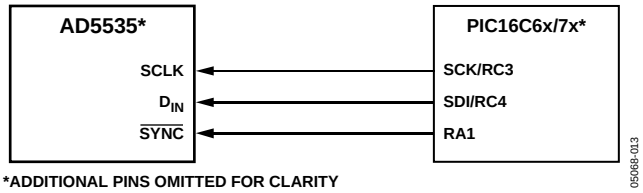

Figure 13. AD5535 to PIC16C6x/7x Interface

AD5535 to 8051

The AD5535 requires a clock synchronized to the serial data. The 8051 serial interface must, therefore, be operated in Mode 0. In this mode, serial data exits the 8051 through RxD, and a shift clock is output on TxD. The $\overline{\text{SYNC}}$ signal is derived from a port line (P1.1). Figure 14 shows how the 8051 is connected to the AD5535. Because the AD5535 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. Note also that the AD5535 requires its data with the MSB first. Because the 8051 outputs the LSB first, the transmit routine must take this into account.

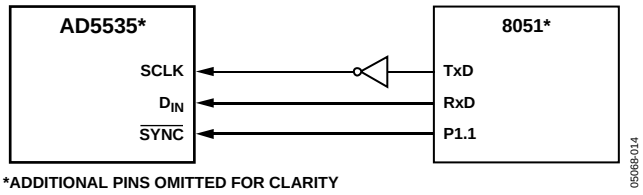

Figure 14. AD5535 to 8051 Interface

APPLICATIONS INFORMATION

MEMS MIRROR CONTROL APPLICATION

The AD5535 is targeted to all optical switching control systems based on micro-electromechanical systems (MEMS) technology. The AD5535 is a 32-channel, 14-bit DAC with integrated high voltage amplifiers. The output amplifiers are capable of generating an output range of 0 V to 200 V when using a 4 V reference. The full-scale output voltage is programmable from 50 V to 200 V using reference voltages from 1 V to 4V. Each amplifier can output 700 µA and directly drives the control actuators, which determine the position of MEMS mirrors in optical switch applications.

The AD5535 is generally used in a closed-loop feedback system, as shown in Figure 15, with a high resolution ADC and DSP. The exact position of each mirror is measured using capacitive sensors. The sensor outputs are multiplexed using an ADG739 to an 8-channel 14-bit ADC (AD7856). An alternative solution is to multiplex using a 32-to-1 multiplexer (ADG732) into a single-channel ADC (AD7671). The control loop is driven by an ADSP-21065L, a 32-bit SHARC DSP with an SPI-compatible SPORT interface. With its 14-bit monotonic behavior and 0 V to 200 V output range coupled with its fast serial interface, the AD5535 is ideally suited for controlling a cluster of MEMS-based mirrors.

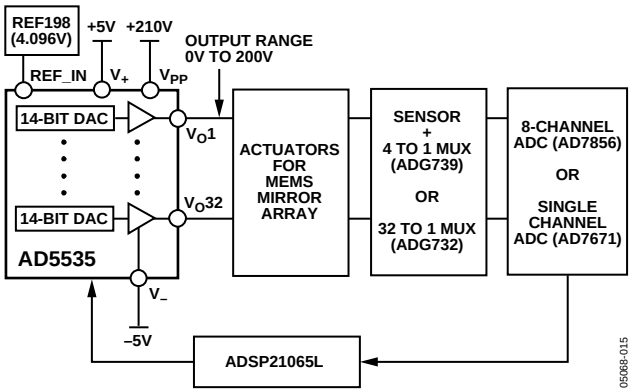

Figure 15. AD5535 in a MEMS-Based Optical Switch

AD5535 BOARD LAYOUT TO ENSURE COMPLIANCE WITH IPC-221 SPECIFICATION

The diagram in Figure 16 is a typical 2-layer printed circuit board layout for the AD5535 complying with the specifications outlined in IPC221. The four corner balls labeled as original no-connects must remain, because no connections and no signals should be connected to these balls. Balls labeled as additional no-connects should be connected to AGND.

The routing shown in Figure 16 shows the feasibility of connecting to the high voltage balls while complying with the spacing requirements of IPC-221. Figure 17 shows the physical distances that are available.

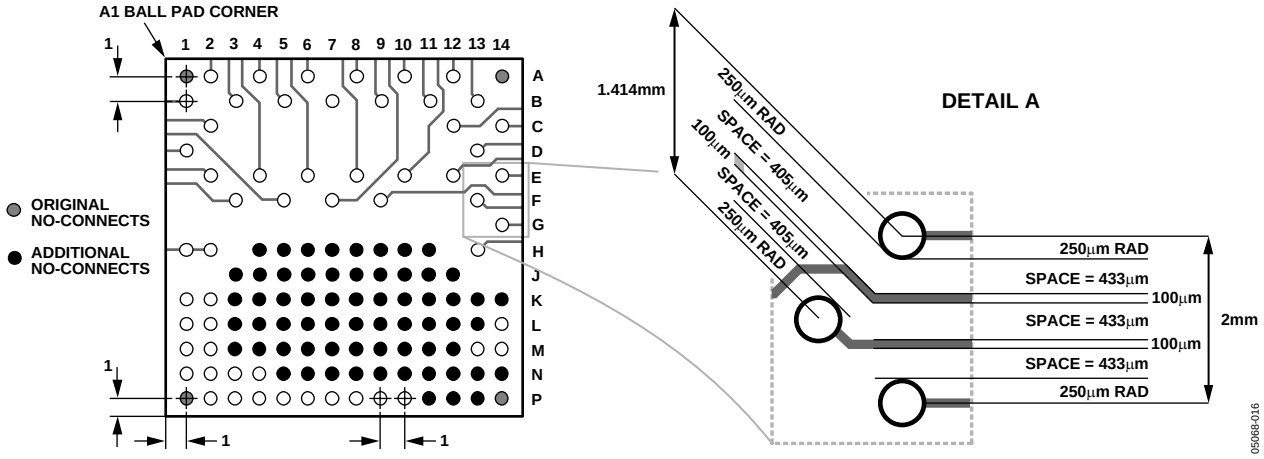

Figure 16. Layout Guidelines to Comply with IPC-221

POWER SUPPLY SEQUENCING AND DECOUPLING RECOMMENDATIONS

The diagram in Figure 17 shows the recommended decoupling, and power supply protection for the AD5535. On the AD5535 it is recommended that all grounds be tied together as close to the device as possible. All supplies should be brought back separately and a provision be made on the board via a link option to drive the AV_{CC} and V_+ from the same supply if required to reduce the number of supplies. All power supplies should be adequately decoupled with 10 uF tantalum and 0.1 uF ceramic capacitors. Note that the capacitors on the V_{PP} supply must be rated at greater than 210 V. To overcome issues associated with power supply sequencing when using high voltage supplies, the use of protection diodes as indicated in Figure 17 is recommended.

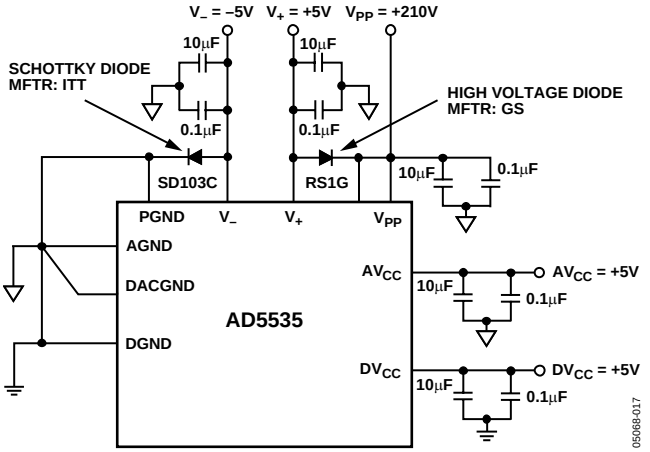

Figure 17. Recommended Power Supply Sequencing and Decoupling

GUIDELINES FOR PRINTED CIRCUIT BOARD LAYOUT

Printed circuit boards should be designed such that the analog and digital sections are separated and confined to designated analog and digital sections of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally found to be the best for ground planes, because this optimizes shielding of sensitive signal lines. Digital and analog grounds planes should be joined only in one place, at the AGND and DGND pins of the high resolution converter. Data and address busses on the board should be buffered or latched to isolate the high frequency bus of the processor from the bus of the high-resolution converters. These act as a faraday shield and increase the signal-to-noise performance of the converters by reducing the amount of high frequency digital coupling. Avoid running digital lines under the device, because they couple noise onto the die. The ground plane should be allowed to run under the IC to avoid noise coupling.

As large a trace as possible should be used for the supply lines to the device to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near analog inputs of devices. Avoid crossovers of digital and analog signals. Traces for analog inputs should be kept as wide and as short as possible and should be shielded with analog ground where possible. Traces on opposite sides of a 2-layer printed circuit board should run at right angles to each other to reduce the effects of feedthrough through the board.

A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique the component side of the board is dedicated to ground planes, and signals are placed on the solder side. Multilayer printed circuit boards with dedicated ground, power, and tracking layers offer the optimum solution in terms of obtaining analog performance but at increased manufacturing costs.

Good decoupling is vitally important when using high resolution converters. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF ceramic capacitors to analog ground. To achieve the best from the decoupling components, these have to be placed as close to the device as possible ideally right up against the IC or IC socket. The main aim of a bypassing element is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. By keeping the decoupling as close to the device as possible, the loop area is kept as small as possible, thereby reducing the possibility of power-supply spikes. Digital supplies of high resolution converters should be decoupled with 10 µF tantalum and 0.1 µF ceramic to the digital ground plane. VDD and VSS supplies of amplifiers should be decoupled again with 10 µF and 0.1 µF to AGND.

All logic chips should be decoupled with 0.1µF to digital ground to decouple high frequency effects associated with digital circuitry.

OUTLINE DIMENSIONS

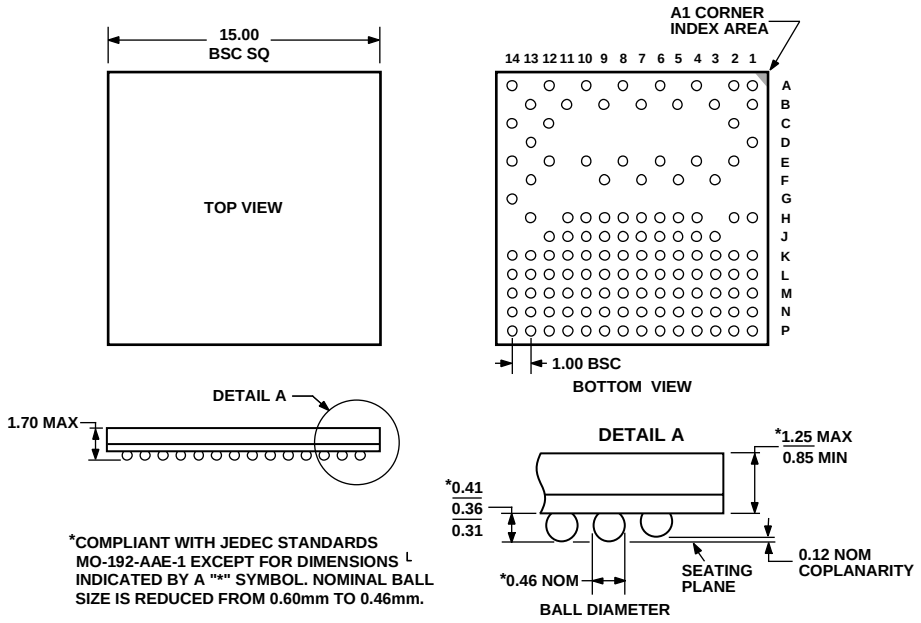

Figure 18. 124-Lead CSB-BGA Package [CSP-BGA]
(BC-124)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Function	Output Voltage Span	Temperature Range	Package Description	Package Option
AD5535ABC	32 DACs	0 to 200 V maximum	−10°C to +85°C	124-Lead CSP-BGA	BC-124

NOTES

PR05068–0–10/04(PrE)